**Scenario: Data Cache hit/miss of a particular set(0xC240)**

0 0x003C2400

1 0x800C2410

1 0x003C2400

0 0x003C240E

0 0x888C242F

1 0x800C2410

0 0xEDAC240B

Note: All cache line are initialized as invalid state. First write is write through so the state goes to valid instead of modified

Step1: 0 0x003C2400-Read operation-Read Miss(Unoccupied)

Binary Representation of 0x003C2400 is 0000 0000 0011 1100 0010 0100 0000 0000

In which:

* Byte offset: 000000
* Set bit: 1100 0010 0100 00 (0xC240)
* Tag bit: 0000 0000 0011(0x003)
* Load to way 0 with tag 003. This line become Valid state, and this become the MRU

Way-0 Way-1 Way-2 Way-3

003

Index

LRU 3 -1 -1 -1

State V I I I

Step 2: 1 0x800C2410-Write Operation-Write Miss(Unoccupied)

Binary Representation of 0x800C2410 is 1000 0000 0000 1100 0010 0100 0001 0000

In which:

* Byte offset: 01 0000
* Set bit: 1100 0010 0100 00 (0xC240)
* Tag bit: 1000 0000 0000 (0x800)
* First write is the write through so the state goes to Valid instead of modified

Way-0 Way-1 Way-2 Way-3

003

800

Index

LRU 2 3 -1 -1

State V V I I

Step 3: 1 0x003C2400-Write Operation -> **Write hit**

Binary Representation of 0x003C2400 is 0000 0000 0011 1100 0010 0100 0000 0000

In which:

* Byte offset: 01 0000
* Set bit: 1100 0010 0100 00 (0xC240)
* Tag bit: 1000 0000 0000 (0x800)
* Write hit occurs not the first write -> so the state will become Modified state, it will update to MRU

Way-0 Way-1 Way-2 Way-3

003

800

Index

LRU 3 2 -1 -1

State M V I I

Step 4: 0 0x003C240E-Read Operation -> **Read Hit**

Binary Representation of 0x003C240E is 0000 0000 0011 1100 0010 0100 0000 1110

In which:

* Byte offset: 00 1110
* Set bit: 1100 0010 0100 00 (0xC240)
* Tag bit: is 0000 0000 0011 (0x003)
* Different byte offset does not mean cache miss
* Read hit into Modified state does not change state

Way-0 Way-1 Way-2 Way-3

003

800

Index

LRU 3 2 -1 -1

State M V I I

Step 5: 0 0x888C242F-Read Operation – Read Miss

Binary Representation of 888C242F is 1000 1000 1000 1100 0010 0100 0010 1111

In which:

* Byte offset: 10 1111
* Set bit: 1100 0010 0100 00(0xC240)
* Tag bit: is 1000 1000 1000 (0x888)
* Read miss -> Loads to way 2 with 0x888

Way-0 Way-1 Way-2 Way-3

003

800

888

Index

LRU 2 1 3 -1

State M V V I

Step 6: 1 0x800C2410-Write Operation-**Write Hit**

Binary Representation of 0x800C2410 is 1000 0000 0000 1100 0010 0100 0001 0000

In which:

* Byte offset: 01 0000
* Set bit: 1100 0010 0100 00 (0xC240)
* Tag bit: 1000 0000 0000 (0x800)
* Write hit occurs in line Valid so it becomes Modified state

Way-0 Way-1 Way-2 Way-3

003

800

888

Index

LRU 1 3 2 -1

State M M V I

Step 7: 0 0xEDAC240B-Read Opearation-**Read Miss**

Binary Representation of 0xEDAC240B is 1110 1101 1010 1100 0010 0100 0000 1011

In which:

* Byte offset: 00 1011
* Set bit: 1100 0010 0100 00 (0xC240)
* Tag bit: 1110 1101 1010 (0xEDA)
* Read Miss occurs -> loads to way 3 -> become the Valid line and MRU

Way-0 Way-1 Way-2 Way-3

EDA

003

800

888

Index

LRU 0 2 1 3

State M M V V

**Scenario: Data Cache hit/miss of a particular set(0xC240)**

3 0x888C242F

0 0x666C243E

1 0x696C241A

Note:

* When evicted data of a line, there is no need to update LRU
* Cache Miss occurs when the line is full, it will evict the way has LRU = 0 to replace

Step 1: 3 0x888C242F-Evict command from L2 for L1

Binary Representation of 888C242F is 1000 1000 1000 1100 0010 0100 0010 1111

In which:

* Byte offset: 10 1111
* Set bit: 1100 0010 0100 00(0xC240)
* Tag bit: is 1000 1000 1000 (0x888)
* Evict data of way-2 and reset the state to Invalid. No need to change LRU state

Way-0 Way-1 Way-2 Way-3

EDA

003

800

Index

LRU 0 2 1 3

State M M I V

Step 2: 0 0x666C243E-Read Operation-Read Misss

Binary Representation of 0x666C243E is 0110 0110 0110 1100 0010 0100 0011 1110

In which:

* Byte offset: 11 1110
* Set bit: 1100 0010 0100 00 (0xC240)
* Tag bit: is 0110 0110 0110 (0x666)
* Here an empty way in the set, so way-2 is preferred instead of replacing way-0 with LRU 0
* The line with LRU value greater than 1 will decremented

Way-0 Way-1 Way-2 Way-3

EDA

003

800

666

Index

LRU 0 1 3 2

State M M V V

Step 3: 1 0x696C241A- Write Operation- Write Miss

Binary Representation of 0x696C241A is 0110 1001 0110 1100 0010 0100 0001 1010

In which:

* Byte offset: 01 1010
* Set bit: 1100 0010 0100 00 (0xC240)
* Tag bit: is 0110 1001 0110 (0x696)
* Way-0 is evicted because LRU = 0, and now the line is in Modified state. So this modified content in this line is written back to the memory before implementing Read block from L2
* After write back the line become Invalid. So when the address write to Invalid line it become Valid state

Way-0 Way-1 Way-2 Way-3

EDA

696

800

666

Index

LRU 3 0 2 1

State V M V V